Chettinad College of Engineering & Technology

Department of Electronics and Communication Engineering

Ec8691-Microprocessors and Microcontrollers

UNIT II 8086 SYSTEM BUS STRUCTURE

MCQ BANK

1. Which of the following is not a Features of 8086?
   A. It uses two stages of pipelining
   B. It is available in 3 versions based on the frequency of operation
   C. Fetch stage can prefetch up to 6 bytes of instructions
   D. It has 512 vectored interrupts.
   ANSWER:D. It has 512 vectored interrupts.

2. 8086 can access up to?
   A. 512KB
   B. 1Mb
   C. 2Mb
   D. 256KB
   ANSWER:B. 1Mb

3. It is an edge triggered input, which causes an interrupt request to the microprocessor.
   A. NMI
   B. INTR
   C. INTA
   D. ALE
   ANSWER:A. NMI

4. How many types of Interfacing are there in microprocessor?
   A. 2
   B. 3
   C. 4
   D. 5
   ANSWER:A. 2

5. In which mode, the CPU periodically reads an internal flag of 8279 to check whether any key is pressed or not with key pressure?

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A. Interrupt mode
B. Polled mode
C. Decoded Mode
D. Encoded Mode
ANSWER:B. Polled mode

6. What is true about Encoded Mode?
   A. the unit contains registers to store the keyboard, display modes
   B. the counter internally decodes the least significant 2 bits and provides a decoded 1 out of 4 scan on SL0-SL3.
   C. the processor is requested service only if any key is pressed, otherwise the CPU will continue with its main task.
   D. the counter provides the binary count that is to be externally decoded to provide the scan lines for the keyboard and display.
   ANSWER:D. the counter provides the binary count that is to be externally decoded to provide the scan lines for the keyboard and display

7. Which pin is used to blank the display during digit switching?
   A. WR
   B. IR
   C. BD
   D. DB
   ANSWER:C. BD

8. DMA stands for?
   A. Display Memory Access
   B. Directly Memory Access
   C. Device Memory Access
   D. Direct Memory Access
   ANSWER:D. Direct Memory Access

9. Which of the following is not true features of 8257?
   A. It has three channels which can be used over three I/O devices.
   B. Each channel has 16-bit address and 14-bit counter.
   C. Each channel can transfer data up to 64kb.
   D. Each channel can be programmed independently.
   ANSWER:A. It has three channels which can be used over three I/O devices

10. What is correct range of frequency for 8257?

A. 500Hz to 3MHz.
B. 250Hz to 2MHz.
C. 250Hz to 3MHz.
D. 500Hz to 2MHz.
ANSWER:C. 250Hz to 3MHz.

11. The processors used in the multi-microprocessor are
A. coprocessors
B. independent processors
C. coprocessors or independent processors
D. none of the mentioned
ANSWER:C. coprocessors or independent processors

12. In tightly coupled systems, the microprocessors share
A. common clock
B. bus control logic
C. common clock and bus control logic
D. none of the mentioned
ANSWER:C. common clock and bus control logic

13. The loosely coupled system has an advantage of
A. more number of CPUs can be added
B. system structure is modular
C. more fault-tolerant and suitable for parallel applications
D. all of the mentioned
ANSWER:D. all of the mentioned

14. To indicate the completion of task allocated in a closely (tightly) coupled system, the microprocessor uses
A. status bit in memory
B. interrupts the host
C. status bit in memory or interrupts the host
D. clock pulse
ANSWER:C. status bit in memory or interrupts the host

15. The stage in which the CPU fetches the instructions from the instruction cache in superscalar organization is
A. Prefetch stage
B. D1 (first decode) stage

C. D2 (second decode) stage
D. Final stage
ANSWER:A. Prefetch stage

16. The CPU decodes the instructions and generates control words in
A. Prefetch stage
B. D1 (first decode) stage
C. D2 (second decode) stage
D. Final stage
ANSWER:B. D1 (first decode) stage

17. The fifth stage of pipeline is also known as
A. read back stage
B. read forward stage
C. write back stage
D. none of the mentioned
ANSWER:C. write back stage

18. In the execution stage the function performed is
A. CPU accesses data cache
B. executes arithmetic/logic computations
C. executes floating point operations in execution unit
D. all of the mentioned
ANSWER:D. all of the mentioned

19. The feature of separated caches is
A. supports the superscalar organization
B. high bandwidth
C. low hit ratio
D. all of the mentioned
ANSWER:D. all of the mentioned

20. In the operand fetch stage, the FPU (Floating Point Unit) fetches the operands from
A. floating point unit
B. instruction cache
C. floating point register file or data cache
D. floating point register file or instruction cache
ANSWER:C. floating point register file or data cache

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21. Example of an external interrupt is
    A. divide by zero interrupt
    B. keyboard interrupt
    C. overflow interrupt
    D. type2 interrupt
    ANSWER:B. keyboard interrupt

22. If 'n' denotes the number of clock cycles and 'T' denotes period of the clock at which the microprocessor is running, then the duration of execution of loop once can be denoted by
    A. n+T
    B. n-T
    C. n*T
    D. n/T
    ANSWER:C. n*T

23. The number of instructions actually executed by the microprocessor depends on the
    A. stack
    B. loop count
    C. program counter
    D. time duration
    ANSWER: B. loop count

24. If there are 'n' case of subroutines, the actual number of instructions executed by the processor depends on
    A. loop count
    B. length of interrupt service routine
    C. length of procedure
    D. none
    ANSWER:C. length of procedure

25. The Count, N can be defined as
    A. required delay/duration for execution
    B. duration of execution/required delay
    C. required delay/number of clock cycles
    D. required delay/period of clock frequency
    ANSWER:A. required delay/duration for execution

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